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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,500	11/06/2001	Ravi Kumar DVJ	P04950 (NAT115-04950)	6797

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Docket Clerk
P.O. Drawer 800889
Dallas, TX 75380

EXAMINER
KINKEAD, ARNOLD M

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,500	DVJ, RAVI KUMAR	
	Examiner	Art Unit	
	Arnold M Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 February 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other:

DETAILED ACTION

Drawings

The formal drawings have been received 02-24-03.

Specification

1. The disclosure is objected to because of the following informalities: In the disclosure a number of values including " W,V,J,U,T,Q,P, K, and S" are provided but they have not been defined, please clarify.

2. On page 7, lines 3 and 9, " M is in the range" should read—N is in the range--.

3. Please specify corresponding co-pending applications for the docket numbers provided in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2,3,4,5,6,7,8,9,11,12,13,14,16,17,18,19,20,21,22,23, 25,26,27, and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the claims above particular ranges have been set however it is not clear what the particular range values such as " W,V,J,U,T,Q,P, K, and S" represent in the particular ranges for the divider values M and N. What is the relationship between the range values?

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 IS rejected under 35 U.S.C. 102(b) as being anticipated by Llewellyn(US 5,339,050).

The reference by Llewellyn discloses a PLL synthesizer(see figure 2 and col. 5, lines 15-31) which comprises a VCO(210) that receives a control voltage stored on loop filter(209); the vco generates an output clock signal(Fout) determined by the control voltage. A first frequency divider(206) divides the output clock signal to produce a first divided clock signal (Fout/M.)

A second frequency divider(202) is shown to divide a reference frequency Fin by a second divider value N to produce a second divided clock signal (Fin/N.)

A phase – frequency detector(207) is shown for comparing the first and second divided clock signals and generates an UP or DOWN control signal based on the comparison.

A charge pump (208) is shown receiving the UP/DOWN control signals to increase/decrease the frequency control voltage on the loop filter. A loop response circuit including DAC(220) and controller(not shown) allows for the Pump current to be adjusted as a function of the divider values(see col. 5, lines 15-31).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10,15 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Llewellyn(US 5,339,050) and further in view of Davis et al (US 5,420,545).

The reference by Llewellyn discloses a PLL synthesizer(see figure 2 and col. 5, lines 15-31) which comprises a VCO(210) that receives a control voltage stored on loop filter(209); the vco generates an output clock signal(Fout) determined by the control voltage. A first frequency divider(206) divides the output clock signal to produce a first divided clock signal (Fout/M.)

A second frequency divider(202) is shown to divide a reference frequency Fin by a second divider value N to produce a second divided clock signal (Fin/N.)

A phase – frequency detector(207) is shown for comparing the first and second divided clock signals and generates an UP or DOWN control signal based on the comparison.

A charge pump (208) is shown receiving the UP/DOWN control signals to increase/decrease the frequency control voltage on the loop filter. A loop response circuit including DAC(220) and controller(not shown) allows for the Pump current to be adjusted as a function of the divider values(see col. 5, lines 15-31).

The reference does not show control of the resistance in the loop filter(claims 10, and 24) with the divider value changes, however, this is a conventional PLL

LPFcontrol and will be highlighted in the Davis et al reference. The reference also does not describe an integrated circuit for the PLL and a processor operating at a plurality of clock speeds(claim 15). With regards the last two items, integration of these PLL circuits is common practice due to the advances and requirements made in the field. The integration of the PLL elements allow for a more compact package and easier process control as the elements can be fabricated with similar characteristics on each IC substrate. With regards a processor operating at a plurality of clock speeds. these PLL' s are used in communication systems and networks and serve to synchronize processors either local or remote that operate with a number of clock signals; these are conventional and official notice is taken.

With regards the Davis et al reference, figures 1 and 2 dislcose a PLL(10) which comprises a loop filter(see figure 2) whereby as noted in cols. 3-4, in fastlock mode the dividers are changed and also, the loop filter resistance is also changed as a consequence of the dividers being changed so as to allow for a quicker lock response.

In light of the above it would have been obvious for one of ordinary skill in the art at the time of the invention to realize that the PLL of Llewellyn could be implemented as integrated device, this allowing for a compact and more stable PLL circuit. The use of such circuits in networks with processors running at different clock speeds for synchronizing is conventional and official notice is taken here. The PLL allows for proper synchronization of such a processor(s). The Davis et al reference serves to highlight the fact that the loop filter is a factor when the divider values are changed to allow for quicker loop response and thus faster lock times, this in addition to pump current control would be part of the Llewellyn PLL to provide a more rapid synchronization which is desireable.

Allowable Subject Matter

10. Claims 2-9,11-14,16-23, and 25-28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. The examiner could not find fair suggestion in the prior art for the relationships between pump current levels and divider values,i.e., setting Ic to minimum and other current levels when N is in a range...or setting the resistance R based on the dividers being in a range....

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 703-305-3486. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 703-308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
June 2, 2003